IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: **WUIDART**

Serial No. **Not Yet Assigned**

Filing Date: **Herewith**

For: **SECURED MICROPROCESSOR COMPRISING A SYSTEM FOR ALLOCATING RIGHTS TO LIBRARIES**

I HEREBY CERTIFY THIS PAPER OR FEE IS BEING DEPOSITED WITH THE U.S. POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED BELOW AND IS ADDRESSED TO: BOX PATENT APPLICATIONS, ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231.

EXPRESS MAIL NO: EL747059127US

DATE OF DEPOSIT: June 20, 2001

NAME: Kyle Hopkinson

SIGNATURE:

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Drawings:

Submitted herewith is a request for a proposed drawing modifications to add missing reference labels to FIG. 3 as indicated in red ink.

In the Claims:

Please cancel Claims 1 to 10.

Please add new Claims 11 to 42.

11. A secured microprocessor device comprising: a microprocessor, an address bus, and a memory array

connected to said microprocessor by said address bus, said memory array divided into a plurality of memory zones; and

a rights allocation system cooperating with said microprocessor and said memory array for allocating, to programs executable by said microprocessor, permanent rights of access to at least one memory zone, said rights allocation system including a rights allocation table having first and second inputs and receiving, at the first input, an identification code of a program or of a sub-program and, at the second input, an identification code of memory zones designated by a current address on said address bus;

said rights allocation system being arranged to confer, on a sub-program shared by at least two programs, temporary rights of access to at least one memory zone when the sub-program is called by one of the at least two programs, and said rights allocation system comprising first input means for applying, to the first input of the rights allocation table, during execution of the sub-program, an identification code of the program having called the sub-program.

12. A secured microprocessor device according to Claim 11, wherein said rights allocation system comprises means to temporarily confer rights of the calling program on the sub-program.

13. A secured microprocessor device according to Claim 11, wherein said rights allocation system comprises means to confer permanent rights on the sub-program that are independent of those of the calling program.

14. A secured microprocessor device according to

Claim 11, wherein said rights allocation system comprises means for simultaneously applying, to the first input of the rights allocation table, during execution of the sub-program, an identification code of the sub-program being executed and the identification code of the program having called the sub-program.

15. A secured microprocessor device according to Claim 14, wherein said first input means comprises a logic device; and wherein bits of the identification code of the sub-program being executed and bits of the identification code of the program having called the sub-program are combined by said logic device before being applied to the first input of the rights allocation table.

16. A secured microprocessor device according to Claim 11, wherein said rights allocation system comprises:

a first latch for storing, during execution of an instruction, an identification code of the program or sub-program being executed; and

a second latch, having an input connected to an output of said first latch, for storing the identification code of the program being executed when said microprocessor switches to the sub-program, and for forming the identification code of the program that called the sub-program, with said second latch being reset when said microprocessor exits from the sub-program.

17. A secured microprocessor device according to Claim 16, wherein said rights allocation system further comprises a first address decoder connected to said address

bus; and wherein loading and resetting of said second latch is controlled by said first address decoder receiving current addresses on said address bus, and for applying a loading signal to said second latch when an address of a first instruction of the sub-program is detected, and for delivering a resetting signal to said second latch when an address of a last instruction of the sub-program is detected.

18. A secured microprocessor device according to Claim 16, wherein said rights allocation system further comprises a second address decoder connected to said address bus; and wherein the identification codes of the memory zones designated by current addresses and the identification codes of the programs and sub-programs being executed are delivered by said second address decoder receiving the current addresses on said address bus.

19. A secured microprocessor device according to Claim 11, wherein said rights allocation system generates an address violation signal when an address on said address bus does not correspond to rights permanently or temporarily allocated to the program or sub-program being executed.

20. A secured microprocessor device according to Claim 19, further comprising an interrupt decoder connected to said rights allocation system; and wherein the address violation signal is processed by said interrupt decoder for causing said microprocessor to execute an address violations processing sub-program.

21. A secured microprocessor device comprising:

a microprocessor, an address bus, and a memory array connected to said microprocessor by said address bus, said memory array divided into a plurality of memory zones; and

a rights allocation system cooperating with said microprocessor and said memory array for allocating, to programs executable by said microprocessor, permanent rights of access to at least one memory zone, said rights allocation system including a rights allocation table having first and second inputs and receiving, at the first input, an identification code of a program or of a sub-program and, at the second input, an identification code of memory zones designated by a current address on said address bus;

said rights allocation system being arranged to confer, on a sub-program shared by at least two programs, temporary rights of access to at least one memory zone when the sub-program is called by one of the at least two programs.

22. A secured microprocessor device according to Claim 21, wherein said rights allocation system comprises a logic device for applying, to the first input of the rights allocation table, during execution of the sub-program, an identification code of the program having called the sub-program.

23. A secured microprocessor device according to Claim 21, wherein said rights allocation system comprises means to temporarily confer rights of the calling program on the sub-program.

24. A secured microprocessor device according to Claim 21, wherein said rights allocation system comprises

means to confer permanent rights on the sub-program that are independent of those of the calling program.

25. A secured microprocessor device according to Claim 21, wherein said rights allocation system comprises means for simultaneously applying, to the first input of the rights allocation table, during execution of the sub-program, an identification code of the sub-program being executed and the identification code of the program having called the sub-program.

26. A secured microprocessor device according to Claim 25, wherein bits of the identification code of the sub-program being executed and bits of the identification code of the program having called the sub-program are combined by said logic device before being applied to the first input of the rights allocation table.

27. A secured microprocessor device according to Claim 21, wherein said rights allocation system comprises:

a first latch for storing, during execution of an instruction, an identification code of the program or sub-program being executed; and

a second latch, having an input connected to an output of said first latch, for storing the identification code of the program being executed when said microprocessor switches to the sub-program, and for forming the identification code of the program that called the sub-program, with said second latch being reset when said microprocessor exits from the sub-program.

28. A secured microprocessor device according to Claim 27, wherein said rights allocation system further comprises a first address decoder connected to said address bus; and wherein loading and resetting of said second latch is controlled by said first address decoder receiving current addresses on said address bus, and for applying a loading signal to said second latch when an address of a first instruction of the sub-program is detected, and for delivering a resetting signal to said second latch when an address of a last instruction of the sub-program is detected.

29. A secured microprocessor device according to Claim 27, wherein said rights allocation system further comprises a second address decoder connected to said address bus; and wherein the identification codes of the memory zones designated by current addresses and the identification codes of the programs and sub-programs being executed are delivered by said second address decoder receiving the current addresses on said address bus.

30. A secured microprocessor device according to Claim 21, wherein said rights allocation system generates an address violation signal when an address on said address bus does not correspond to rights permanently or temporarily allocated to the program or sub-program being executed.

31. A secured microprocessor device according to Claim 30, further comprising an interrupt decoder connected to said rights allocation system; and wherein the address violation signal is processed by said interrupt decoder for causing said microprocessor to execute an address violations

processing sub-program.

32. A method for sharing a sub-program by at least two programs within a secured microprocessor device comprising a microprocessor, an address bus, and a memory array connected to the microprocessor by the address bus, the memory array divided into a plurality of memory zones, and a rights allocation system cooperating with the microprocessor and the memory array, the method comprising:

allocating, to programs executable by the microprocessor, permanent rights of access to at least one memory zone, the rights allocation system including a rights allocation table having first and second inputs and receiving, at the first input, an identification code of a program or of a sub-program and, at the second input, an identification code of memory zones designated by a current address on the address bus;

the rights allocation system being arranged to confer, on a sub-program shared by at least two programs, temporary rights of access to at least one memory zone when the sub-program is called by one of the at least two programs.

33. A method according to Claim 32, wherein the rights allocation system comprises a logic device for applying, to the first input of the rights allocation table, during execution of the sub-program, an identification code of the program having called the sub-program.

34. A method according to Claim 32, wherein the rights allocation system comprises means to temporarily confer rights of the calling program on the sub-program.

35. A method according to Claim 32, wherein the rights allocation system comprises means to confer permanent rights on the sub-program that are independent of those of the calling program.

36. A method according to Claim 32, wherein the rights allocation system comprises means for simultaneously applying, to the first input of the rights allocation table, during execution of the sub-program, an identification code of the sub-program being executed and the identification code of the program having called the sub-program.

37. A method according to Claim 36, wherein bits of the identification code of the sub-program being executed and bits of the identification code of the program having called the sub-program are combined by the logic device before being applied to the first input of the rights allocation table.

38. A method according to Claim 32, wherein the rights allocation system comprises:

a first latch for storing, during execution of an instruction, an identification code of the program or sub-program being executed; and

a second latch, having an input connected to an output of the first latch, for storing the identification code of the program being executed when the microprocessor switches to the sub-program, and for forming the identification code of the program that called the sub-program, with the second latch being reset when the microprocessor exits from the sub-program.

39. A method according to Claim 38, wherein the rights allocation system further comprises a first address decoder connected to the address bus; and wherein loading and resetting of the second latch is controlled by the first address decoder receiving current addresses on the address bus, and for applying a loading signal to the second latch when an address of a first instruction of the sub-program is detected, and for delivering a resetting signal to the second latch when an address of a last instruction of the sub-program is detected.

40. A method according to Claim 38, wherein the rights allocation system further comprises a second address decoder connected to the address bus; and wherein the identification codes of the memory zones designated by current addresses and the identification codes of the programs and sub-programs being executed are delivered by the second address decoder receiving the current addresses on the address bus.

41. A method according to Claim 32, wherein the rights allocation system generates an address violation signal when an address on the address bus does not correspond to rights permanently or temporarily allocated to the program or sub-program being executed.

42. A method according to Claim 41, further comprising an interrupt decoder connected to the rights allocation system; and wherein the address violation signal is processed by the interrupt decoder for causing the microprocessor to execute an address violations processing

sub-program.

REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner's convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability. Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
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EXPRESS MAIL NO: EL747059127US

DATE OF DEPOSIT: June 20, 2001

NAME: Kyle Hopkinson

SIGNATURE:

SUBMISSION OF PROPOSED MODIFICATIONS TO DRAWINGS

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Submitted herewith is a request for a proposed drawing modifications to add missing reference labels to FIG. 3 as indicated in red ink.

Respectfully submitted,

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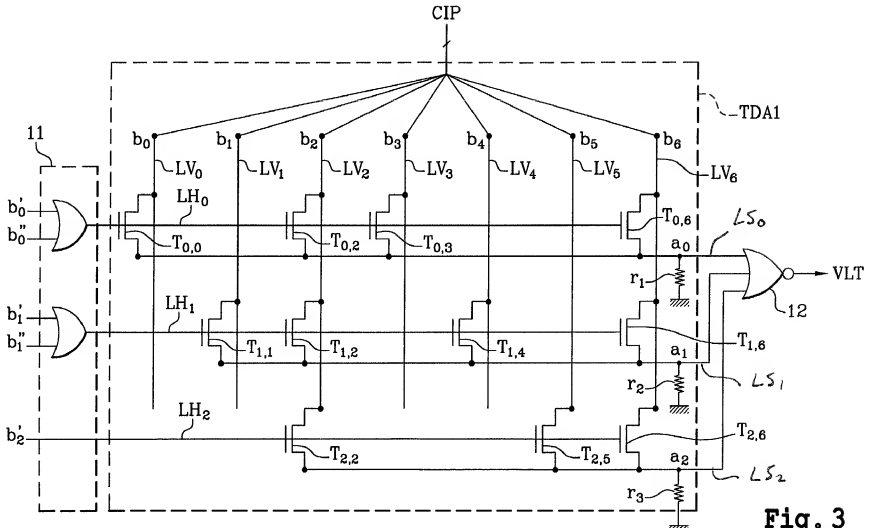
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12
VLT

Fig. 3